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Behavior of Low Power Flash Devices" chapter of the ProASIC3 FPGA Fabric User's Guide for information on clock and lock recovery. Internal Power-Up Activation Sequence 1. Core 2. Input buffers Output buffers, after 200 ns delay from input buffer activation Revision 4 2-5 SmartFusion DC and Switching Characteristics $VCC = VCC_{xxxx}IOBx + VT$

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